Customer No.: 31561
Application No.: 10/711,568
Docket No.:13216-US-PA

AMENDMENTS

To the Claims:

Please replace all prior versions of claims by the following:

1. (Original) A separated power electro-static discharge (ESD) protection circuit coupled between a first power line and a second power line, the separated power ESD protection circuit comprising:

a first diode, having an anode and a cathode, wherein the anode is coupled to the first power line;

a first metal-oxide-semiconductor (MOS) transistor, having a gate, a source and a drain, wherein the drain is coupled to the cathode of the first diode and the source is coupled to the second power line; and

a second diode, having an anode and a cathode, wherein the anode is coupled to the second power line, the cathode is coupled to the first power line, the first diode and the first MOS transistor constitute a parasitic silicon-controlled rectifier (SCR) for providing a static discharge route.

2. (Original) The separated power ESD protection circuit of claim 1, further comprising a second MOS transistor having a gate, a source and a drain, wherein the drain is coupled to the cathode of the second diode, the source is coupled to the first power line, and the second diode and the second MOS transistor constitute a parasitic SCR.

3. (Original) The separated power ESD protection circuit of claim 1, wherein the first MOS transistor is an N-type MOS transistor.

4. (Original) The separated power ESD protection circuit of claim 1, wherein the first MOS transistor is a P-type MOS transistor.

5. (Original) The separated power ESD protection circuit of claim 2, wherein the second MOS transistor is an N-type MOS transistor.

6. (Original) The separated power ESD protection circuit of claim 2, wherein the second MOS transistor is a P-type MOS transistor.

7. (Currently amended) A separated power electro-static discharge (ESD) protection circuit coupled between a first power line and a second power line, the separated power ESD protection circuit comprising:

a plurality of first series diodes, each of the first series diodes, having an anode and a cathode, wherein an anode of a first diode of the first series diodes is coupled to a first power line;

a first metal-oxide-semiconductor (MOS) transistor, having a gate, a source and a drain, wherein the drain is coupled to a cathode of a last diode of the first diodes, and the source is coupled to a second power line; and

a plurality of second series diodes, each of the second series diodes having an anode and a cathode, wherein an anode of a first diode of the second series diodes is coupled to the second power line, and [[~~an~~]] a cathode of a last diode of the second series diodes is coupled to the first power line,

wherein the first series diodes and the first MOS transistor constitute a parasitic silicon-controlled rectifier (SCR) for providing a static discharge route.

8. (Original) The separated power ESD protection circuit of claim 7, further comprising a second MOS transistor having a gate, a source and a drain, wherein the drain is coupled to a cathode of a last diode of the second series diodes, the source is coupled to the first power line, and the last diode of the second series diodes and the second MOS transistor constitute a parasitic SCR for providing a static discharge route.

9. (Original) The separated power ESD protection circuit of claim 7, wherein the first MOS transistor is an N-type MOS transistor.

10. (Original) The separated power ESD protection circuit of claim 7, wherein the first MOS transistor is a P-type MOS transistor.

11. (Original) The separated power ESD protection circuit of claim 8, wherein the second MOS transistor is an N-type MOS transistor.

12. (Original) The separated power ESD protection circuit of claim 8, wherein the second MOS transistor is a P-type MOS transistor.

13. (Original) An integrated circuit adapted to protect a first and a second internal circuits from electro-static discharge (ESD), the first internal circuit coupled between a first high power line and a first low power line, the second internal circuit coupled between a second high power line and a second low power line, the first and the second high power lines being separated from each other, the first and the second low power lines being separated from each other, the integrated circuit comprising:

a first ESD protection circuit, coupled between the first high and the first low power lines;

a second ESD protection circuit, coupled between the second high and the second low power lines;

a third ESD protection circuit, coupled between the first high and the second high power lines, selectively grounding the first or the second high power lines while ESD occurring on the

first or the second high power lines, wherein the third ESD protection circuit comprises a first diode string, a first metal-oxide-semiconductor (MOS) transistor and a second diode string, wherein the first diode string and the first MOS transistor are coupled in series; the second diode string are parallel and reverse to the first diode string and the first MOS transistor, and the first diode string and the first MOS transistor constitute a parasitic silicon-controlled rectifier (SCR) for providing a discharge route while triggered by ESD; and

a fourth ESD protection circuit, coupled between the first low and the second low power lines, selectively grounding the first or the second low power lines while ESD occurring on the first or the second low power lines, wherein the fourth ESD protection circuit comprises third diode string, a second metal-oxide-semiconductor (MOS) transistor and fourth diode string, the third diode string and the second MOS transistor are coupled in series; the fourth diode string are parallel reverse to the third diode string and the second MOS transistor; and the third diode string and the second MOS transistor constitute a parasitic silicon-controlled rectifier (SCR) for providing a discharge route while triggered by ESD.

14. (Original) The integrated circuit of claim 13, wherein the first and second MOS transistors comprise an N-type or a P-type MOS transistor.

15. (Original) The integrated circuit of claim 13, wherein first series and second diode string of the third ESD protection circuit comprise at least one diode, and the third series and fourth diode string of the fourth ESD protection circuit comprise at least one diode.

16. (Original) The integrated circuit of claim 15, wherein numbers of the first series and second diode string depend on a voltage difference between the first high power line and the second high power supply bus.

17. (Original) The integrated circuit of claim 15, wherein numbers of the third series and fourth diode string depend on a voltage difference between the first low power line and the second low power supply bus.

18. (Original) The integrated circuit of claim 13, wherein the third ESD protection circuit further comprises a third MOS transistor, which is coupled to the second diode string in series; the first and third MOS transistors are coupled to the second high and the first high power lines, respectively; the fourth ESD protection circuit further comprises a fourth MOS transistor, which is coupled to the fourth diode string in series; and the second and the fourth MOS transistors are coupled to the second and the first low power lines, respectively.

19. (Currently amended) The integrated circuit of claim [[~~16~~]] 18, wherein the first, second, third and fourth MOS transistors comprise an N-type or a P-type MOS transistor.

20. (Original) The integrated circuit of claim 16, further comprising:

a first input ESD protection circuit, coupled and among the first internal circuit, an input pad of the first internal circuit, the first high power line and the first low power line; and

a second input ESD protection circuit, coupled and among the second internal circuit, an input pad of the second internal circuit, the second high power line and the second low power line.